



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE

United States Patent and Trademark Office

Address: COMMISSIONER FOR PATENTS

P.O. Box 1450

Alexandria, Virginia 22313-1450

www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/809,537	03/24/2004	Yosef Solt	MP0345	6150
26200 7590 10/06/2008				
FISH & RICHARDSON P.C.				
P.O BOX 1022				
MINNEAPOLIS, MN 55440-1022				
EXAMINER				
BRADLEY, MATTHEW A				
ART UNIT		PAPER NUMBER		
2187				
NOTIFICATION DATE		DELIVERY MODE		
10/06/2008		ELECTRONIC		

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

PATDOCTC@fr.com

### Office Action Summary

**Application No.**

10/809,537

**Applicant(s)**

SOLT ET AL.

**Examiner**

MATTHEW BRADLEY

**Art Unit**

2187

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 18 June 2008.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-111 is/are pending in the application.
- 4a) Of the above claim(s) 9-17,27-55,65-74,84-93 and 102-110 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-4,18-21,26,56-59,64,75-78,83,94-97 and 111 is/are rejected.
- 7) ☒ Claim(s) 5-8,22-25,60-63,79-82 and 98-101 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-846)
- 3) ☐ Information Disclosure Statement(s) (PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: \_\_\_\_\_

## **DETAILED ACTION**

### ***Response to Amendment***

In view of the Appeal Brief filed on 18 June 2008, PROSECUTION IS HEREBY REOPENED. A new ground(s) of rejection is set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) initiate a new appeal by filing a notice of appeal under 37 CFR 41.31 followed by an appeal brief under 37 CFR 41.37. The previously paid notice of appeal fee and appeal brief fee can be applied to the new appeal. If, however, the appeal fees set forth in 37 CFR 41.20 have been increased since they were previously paid, then appellant must pay the difference between the increased fees and the amount previously paid.

A Supervisory Patent Examiner (SPE) has approved of reopening prosecution by signing below.

### ***Claim Status***

Claims 1-8, 18-26, 56-64, 75-83, 94-101, and 111 remain pending and are ready for examination.

### ***Claim Objections***

Claim 18 is objected to because of the following informalities:

- Claim 18 line 10 recites a period after the word available.

Appropriate correction is required.

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims **1-4, 18-21, 26, 56-59, 64, 75-78, 83, and 111** are rejected under 35 U.S.C. 102(a) and 35 U.S.C. 102(e) as being anticipated by Chen et al (U.S. 2003/0093629), hereinafter referred to as Chen.

As per independent claim **1**, Chen teach, writing one of a plurality of sets in an allocation memory into an allocation register, wherein the allocation memory includes a plurality of data elements arranged in the plurality of sets, each of said data elements being associated with a corresponding plurality of buffers in a buffer memory; (Paragraph 0021: taught as the plurality of bits for controlling a utilization of a bit mask region) in response to an allocation request, identifying a data element in the allocation register having a value corresponding to an available buffer; changing the value of said data element to a value corresponding to an allocated buffer; and allocating the buffer associated with said data element (Paragraph 0020).

As per dependent claim **2**, Chen teach, wherein each of the plurality of data elements comprises a single bit (Paragraph 0016: taught as the bit within the plurality of bits).

As per dependent claim **3**, Chen teach, wherein each of the plurality of sets comprises a line in the allocation memory (Paragraph 0016: taught as the segments of the buffer memory).

As per dependent claim **4**, Chen teach, in response to a clear request for one of the plurality of buffers, identifying a data element associated with said buffer in one of the allocation memory and the allocation register; and changing a value of said data element to the value corresponding to an available buffer (Paragraph 0018: taught as the freeing of occupied memory and making such memory available for future allocation as also shown in Paragraph 0020).

As per dependent claim **111**, Chen teach, wherein each of the plurality of sets is a non-empty set (Paragraph 0016).

As per independent claim **18**, Chen teach, an allocation memory including a plurality of data elements arranged in a plurality of sets, each of said data elements being associated with a corresponding plurality of buffers in a buffer memory; an allocation register; and a buffer manager to write one of said plurality of sets into the allocation register, and in response to an allocation request, identify a data element in the allocation register having a value corresponding, to an available buffer, change the value of said data element to a value corresponding to an allocated buffer, and allocate the buffer associated with said data element (Paragraph 0016 with respect to Figure 5).

*The Examiner incorporates by reference herein the comments made supra with respect to claim 1.*

As per dependent claim **19**, Chen teach, wherein each of the plurality of data elements comprises a single bit (Paragraph 0016: taught as the bit within the plurality of bits).

As per dependent claim **20**, Chen teach, wherein each of the plurality of sets comprises a line in the allocation memory (Paragraph 0016: taught as the segments of the buffer memory).

As per dependent claim **21**, Chen teach, in response to a clear request for one of the plurality of buffers, identifying a data element associated with said buffer in one of the allocation memory and the allocation register; and changing a value of said data element to the value corresponding to an available buffer (Paragraph 0018: taught as the freeing of occupied memory and making such memory available for future allocation as also shown in Paragraph 0020).

As per dependent claim **26**, Chen teach, wherein the allocation memory comprises an SRAM (Paragraph 0017).

As per independent claim **56**, Chen teach, a switching module to receive and switch packets; (Paragraph 0015) a buffer memory including a plurality of buffers to store received packets; and a buffer management module including: an allocation memory including a plurality of data elements arranged in a plurality of sets, each of said data elements being associated with a corresponding one of the plurality of buffers in the buffer memory; an allocation register; and a buffer manager to write one of said

plurality of sets into the allocation register, and in response to an allocation request, identify a data element in the allocation register having a value corresponding to an available buffer, change the value of said data element to a value corresponding to an allocated buffer, and allocate the buffer associated with said data element (Paragraph 0016 with respect to Figure 5). *The Examiner incorporates by reference herein the comments made supra with respect to claim 1.*

As per dependent claim **57**, Chen teach, wherein each of the plurality of data elements comprises a single bit (Paragraph 0016: taught as the bit within the plurality of bits).

As per dependent claim **58**, Chen teach, wherein each of the plurality of sets comprises a line in the allocation memory (Paragraph 0016: taught as the segments of the buffer memory).

As per dependent claim **59**, Chen teach, in response to a clear request for one of the plurality of buffers, identifying a data element associated with said buffer in one of the allocation memory and the allocation register; and changing a value of said data element to the value corresponding to an available buffer (Paragraph 0018: taught as the freeing of occupied memory and making such memory available for future allocation as also shown in Paragraph 0020).

As per dependent claim **64**, Chen teach, wherein the allocation memory comprises an SRAM (Paragraph 0017).

*Claims 75-78 and 83 are interpreted under 35 U.S.C. 112, 6<sup>th</sup> paragraph.*

The Court of Appeals for the Federal Circuit, in its en banc decision *In re Donaldson Co.*, 16 F.3d 1189, 29 USPQ2d 1845 (Fed. Cir. 1994), decided that a "means-or-step-plus-function" limitation should be interpreted in a manner different than patent examining practice had previously dictated. The

Donaldson decision affects only the manner in which the scope of a "means or step plus function" limitation in accordance with 35 U.S.C. 112, sixth paragraph, is interpreted during examination. Donaldson does not directly affect the manner in which any other section of the patent statutes is interpreted or applied.

When making a determination of patentability under 35 U.S.C. 102 or 103, past practice was to interpret a "means or step plus function" limitation by giving it the "broadest reasonable interpretation." Under the PTO's long-standing practice this meant interpreting such a limitation as reading on any prior art means or step which performed the function specified in the claim without regard for whether the prior art means or step was equivalent to the corresponding structure, material or acts described in the specification. However, in Donaldson, the Federal Circuit stated:

Per our holding, the "broadest reasonable interpretation" that an examiner may give means-plus-function language is that statutorily mandated in paragraph six. Accordingly, the PTO may not disregard the structure disclosed in the specification corresponding to such language when rendering a patentability determination. (MPEP 2181)

*Accordingly, the Examiner notes that the means or system/structure for practice of the invention disclosed on pages 4-5 in paragraphs 0011-0012 of Applicant's specification is further taught in Chen from Paragraph 0014 to Paragraph 0017.*

As per independent claim **75**, Chen teach, a switching module including means for receiving and switching packets; a buffer memory including a plurality of buffers for storing received packets; and a buffer management module including: an allocation memory including a plurality of data elements arranged in a plurality of sets, each of said data elements being associated with a corresponding plurality of buffers in a buffer memory; an allocation register; and a buffer manager including means for writing one of said plurality of sets into the allocation register, and means for, in response to an allocation request, identifying a data element in the allocation register having a value corresponding to an available buffer, changing the value of said data element to a value corresponding to an allocated buffer, and allocating the buffer associated with said data element (Paragraph 0016 with respect to Figure 5). *The Examiner incorporates by reference herein the comments made supra with respect to claim 1.*



As per dependent claim **76**, Chen teach, wherein each of the plurality of data elements comprises a single bit (Paragraph 0016: taught as the bit within the plurality of bits).

As per dependent claim **77**, Chen teach, wherein each of the plurality of sets comprises a line in the allocation memory (Paragraph 0016: taught as the segments of the buffer memory).

As per dependent claim **78**, Chen teach, in response to a clear request for one of the plurality of buffers, identifying a data element associated with said buffer in one of the allocation memory and the allocation register; and changing a value of said data element to the value corresponding to an available buffer (Paragraph 0018: taught as the freeing of occupied memory and making such memory available for future allocation as also shown in Paragraph 0020).

As per dependent claim **83**, Chen teach, wherein the allocation memory comprises an SRAM (Paragraph 0017).

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims **94-97** are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen in view of Rubinstein (U.S. 5,913,215).

As per claims **94-97**, claims 94-97 are method versions of claims 1-4

respectively, enabled by instructions rather than hardware. Chen teach a method of a system as discussed *supra* in the rejection of claims 1-4.

Chen, however, does not expressly teach that the method is performed by a software series of instructions, instead disclosing a set of hardware components.

Rubinstein discloses, on Col. 10, lines 3-15, that computer methods may be performed either by a series of instructions, or by specific hardware components that contain hard-wired logic for performing the method, or by any combination of the two.

Chen and Rubinstein are analogous art because they are from the same general field of endeavor, namely computer-controlled methods.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the system of Chen by embodying it in executable instructions.

The motivation for doing so is portability and ease of installation. For example, it is well known that a method encoded in a program may be installed onto different systems much more quickly and easily than can hardware components designed to perform the same method.

Therefore, it would have been obvious to combine Chen with Rubinstein for the benefits shown above, to obtain the invention as specified in claims 94-97.

***Allowable Subject Matter***

Claims 5-8, 22-25, 60-63, 79-82, and 98-101 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

### ***Response to Arguments***

Applicant's arguments, filed 18 June 2008 in the form of an Appeal Brief, have been fully considered and are persuasive. However, upon further consideration, a new ground(s) of rejection is made as noted *supra*. Accordingly, this action has NOT been made final.

Any argument not specifically addressed is considered moot in view of the new ground(s) of rejection.

### ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew Bradley whose telephone number is (571) 272-8575. The examiner can normally be reached on 6:30-3:00 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Ellis can be reached on (571) 272-4205. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

KLE/mb

/Kevin L. Ellis/  
Acting SPE of Art Unit 2187